CLAIMS

I claim:

1. An electronic apparatus comprising:

an insulative substrate comprising an aluminum-based glass; and

a layer comprising a semiconductive material over the substrate.

2. The apparatus of claim 1 further comprising a semiconductor device that includes at least a part of the semiconductive material layer.

3. The apparatus of claim 1 wherein the semiconductive material layer is on and in contact with the insulative substrate.

4. The apparatus of claim 1 wherein the insulative substrate comprises aluminum oxycarbide.

5. The apparatus of claim 1 wherein the insulative substrate exhibits a CTE sufficiently close to a CTE of the semiconductive material layer such that a strain of less than 1% would exist between a 1000 Å thickness of the semiconductive material layer and the insulative substrate.

6. The apparatus of claim 5 wherein the semiconductive material layer has a thickness of about 1000 Å or less.

7. The apparatus of claim 5 wherein the strain would be less than 0.6%.

8. The apparatus of claim 1 wherein the semiconductive material layer comprises monocrystalline silicon.

9. A silicon-on-insulator integrated circuit comprising:

an insulative glass substrate comprising aluminum oxycarbide;

a monocrystalline silicon layer on and in contact with the substrate; and

a semiconductor device comprising at least a part of the silicon layer.

10. The integrated circuit of claim 9 wherein the glass substrate further comprises aluminum carbide, silicon carbide, and α-alumina.

11. The integrated circuit of claim 9 wherein the glass substrate exhibits a CTE sufficiently close to a CTE of the silicon layer such that a strain of less than 1% would exist between a 1000 Å thickness of the silicon layer and the glass substrate.

12. The integrated circuit of claim 11 wherein the silicon layer has a thickness of about 1000 Å or less.

13. The integrated circuit of claim 11 wherein the strain would be less than 0.6%.

14. An electronic apparatus fabrication method comprising:

forming an insulative substrate comprising an aluminum-based glass; and

forming a layer comprising a semiconductive material over the substrate.

15. The method of claim 14 further comprising forming a semiconductor device comprising at least a part of the semiconductive material layer.

16. The method of claim 14 wherein the semiconductive material layer is formed on and in contact with the insulative substrate.

17. The method of claim 14 wherein forming the insulative substrate comprises:

forming a mixture of a powder comprising aluminum, a powder comprising silicon, and a powder comprising carbon;

mechanically activating the mixture and allowing the mixture to react by spontaneous ignition; and

forming the reacted mixture into a plate.

18. The method of claim 17 wherein allowing the mixture to react comprises exposing the mixture to air.

19. The method of claim 17 wherein allowing the mixture to react comprises exposing the mixture to oxygen gas and to an inert gas excluding nitrogen.

20. The method of claim 14 wherein the insulative substrate exhibits a CTE sufficiently close to a CTE of the semiconductive material layer such that a strain of less than 1% would exist between a 1000 Å thickness of the semiconductive material layer and the insulative substrate.

21. The method of claim 20 wherein the semiconductive material layer has a thickness of about 1000 Å or less.

22. The method of claim 20 wherein the strain would be less than 0.6%.

23. The method of claim 14 wherein forming the semiconductive material layer comprises:

removing a layer of silicon from a monocrystalline silicon wafer; and

bonding the silicon layer to the insulative substrate.

24. The method of claim 23 wherein removing the layer of silicon comprises implanting ions into the wafer.

25. The method of claim 23 wherein bonding the silicon layer comprises heating to at least 400 °C.

26. The method of claim 23 wherein bonding the silicon layer comprises laser assisted annealing.

27. The method of claim 23 wherein bonding the silicon layer comprises activating a surface of at least the silicon wafer by exposure to a plasma.

28. The method of claim 14 further comprising chemically-mechanically polishing the semiconductive material layer.

29. A silicon-on-insulator integrated circuit fabrication method comprising:

forming a mixture of a powder comprising aluminum, a powder comprising silicon, and a powder comprising carbon;

mechanically activating the mixture and allowing the mixture to react by spontaneous ignition;

forming the reacted mixture into a glass substrate comprising aluminum oxycarbide;

removing a layer of silicon from a monocrystalline silicon wafer; bonding the silicon layer on and in contact with the glass substrate; and

forming a semiconductor device comprising at least a part of the silicon layer.

30. The method of claim 29 wherein the glass substrate further comprises aluminum carbide, silicon carbide, and α-alumina.

31. The method of claim 29 wherein allowing the mixture to react comprises exposing the mixture to air.

32. The method of claim 29 wherein allowing the mixture to react comprises exposing the mixture to oxygen gas and an inert gas that does not comprise nitrogen.

33. The method of claim 29 wherein the glass substrate exhibits a CTE sufficiently close to a CTE of the silicon layer such that a strain of less than 1% would exist between a 1000 Å thickness of the silicon layer and the glass substrate.

34. The method of claim 33 wherein the silicon layer has a thickness of about 1000 Å or less.

35. The method of claim 33 wherein the strain would be less than 0.6%.

36. The method of claim 29 wherein removing the layer of silicon comprises implanting ions into the wafer.

37. The method of claim 29 wherein bonding the silicon layer comprises heating to at least 400 °C.

38. The method of claim 29 wherein bonding the silicon layer comprises laser assisted annealing.

39. The method of claim 29 further comprising chemically-mechanically polishing the silicon layer after bonding to the glass substrate.

40. A memory device comprising:

an insulative substrate comprising an aluminum-based glass;

a layer comprising a semiconductive material over the substrate; and

a plurality of memory cells that include at least a part of the semiconductive material layer.

41. The memory device of claim 40 wherein the plurality of memory cells comprises an array of memory cells and the memory device comprises DRAM.

42. A memory device comprising:

an insulative glass substrate comprising aluminum oxycarbide;

a monocrystalline silicon layer on and in contact with the substrate; and

a plurality of memory cells that have a capacitor including at least a part of the silicon layer.

43. The memory device of claim 42 wherein the plurality of memory cells comprises an array of memory cells and the memory device comprises DRAM.

44. A computer system, the computer system comprising a memory device and a microprocessor, the memory device including:

an insulative substrate comprising an aluminum-based glass;

a layer comprising a semiconductive material over the substrate; and

a plurality of memory cells that include at least a part of the semiconductive material layer.

45. The computer system of claim 44 wherein the memory device comprises DRAM.

46. A computer system, the computer system comprising a memory device and a microprocessor, the memory device including:

an insulative glass substrate comprising aluminum oxycarbide;

a monocrystalline silicon layer on and in contact with the substrate; and

a plurality of memory cells that have a capacitor including at least a part of the silicon layer.

47. The computer system of claim 46 wherein the memory device comprises DRAM.